

ULSI Workshop 2023 Program (21th May, 2023)

Venue: Small Hall		Presentation No.	Regular Session (15 minutes presentation and 5 minutes Q&A) *Please use your own computer for the presentation.	Names	Affrecaation
Time					
Regular Session	14:30 ~ 14:50	1	Improving Gaussian Elimination-based NNA-compliant Circuit Synthesis Method by Inserting CNOT Gates	Zanhe Qi, Huan YU and Shigeru YAMASHITA	Ritsumeikan University
	14:50 ~ 15:10	2	Improving Steiner-Gauss Elimination by Utilizing Optimized Qubit Layouts	Huan Yu, Zanhe Qi, Shigeru Yamashita	Ritsumeikan University
	15:10 ~ 15:30	3	A new signed-digit addition algorithm	Yuuki Tanaka	Gunma University
	15:30 ~ 15:50	4	Further Acceleration of MLP Training in Systolic Arrays	Takeshi Senoo, Hiroki Nakahara	Tokyo Institute of Technology
Break					
Venue: Small Hall		Poster No.	Poster Short Presentation (2minutes Presentation) *Presentation slides for short presentations should be sent in PDF format in advance.	Names	Affrecaation
Time					
Poster Session	16:10 ~ 16:12	1	Efficient K-RED-Based NTT Accelerator for Crystals-Kyber	Hiroshi Amagasa, Rei Ueno, and Naofumi Homma	Tohoku University
	16:12 ~ 16:14	2	Improvement of the Digital Assisted Current Mirror Using Completely Symmetrical Structure	Shotaro Umemoto, Ryoichi Miyauchi, Keisuke Kondo, Yutaka Fukuchi	Tokyo University of Science
	16:14 ~ 16:16	3	High-precision signal processing using 2nd-order $\Delta \Sigma$ -modulated bitstreams	Akihisa Koyama, Takao Waho, Hitoshi Hayashi	Sophia University
	16:16 ~ 16:18	4	Experimental Evaluation on Anomaly Detection Using Multiple-Valued Decision Trees in an HIS	Shohei Wakasaki Shinobu Nagayama* Masato Inagi Shin'ichi Wakabayashi Rie Kometani Yo Muneta	Hiroshima City University
	16:18 ~ 16:20	5	Further Acceleration of MLP Training in Systolic Arrays	Takeshi Senoo, Hiroki Nakahara	Tokyo Institute of Technology
	16:20 ~ 16:22	6	Experimental Results of Symbol Classification Using Two-dimensional Mapping on FPGA	*Yukihiko Sugiyama, *Yosuke Iijima, **Yasushi Yuminaka	*National Institute of Technology(KOSEN), Oyama college, **Gunma University
	16:22 ~ 16:24	7	Inductor ESR Compensation for LC Analog Filters	*Misaki Takagi, *Takayuki Nakatani, *Shogo Katayama, *Daisuke Iimori, *Gaku Ogihara, *Yujie Zhao, *Syuhei Yamamoto, *Anna Kuwana, **Keno Sato, **Takashi Ishida, **Toshiyuki Okamoto, **Tamotsu Ichikawa, *Kentaroh Katoh, *Kazumi Hatayama, *Yasushi Yuminaka, and *Haruo Kobayashi	*Gunma University, Japan, **ROHM Semiconductor
	16:22 ~ 16:24	8	FFE Coefficient Setting Using Symbol Transition Information of PAM-4 Signals	Nagito Ishida and Yasushi Yuminaka	Gunma University
	16:24 ~ 16:26	9	Improving Output Power of inverse Class-E Amplifiers Using a Current Injection Stage	Ryuji Oka, Akira Hyogo, Tatsuji Matsuura, Ryo Kishida, Ryoichi Miyauchi	Tokyo University of Science
	16:26 ~ 16:28	10	Extremely Low Power Supply Voltage Ring Oscillator Using Stacked Body Bias Inverters	Takeo Furusawa, Tatsuji Matsuura, Ryo Kishida, Ryoichi Miyauchi, Akira Hyogo	Tokyo University of Science
	16:28 ~ 16:30	11	Improvement of power conversion efficiency at low input signal in a cross-coupled differential CMOS rectifier circuit	Tatsumi Hashimoto, Tatsuji Matsuura, Ryo Kishida, Ryoichi Miyauchi, Akira Hyogo	Tokyo University of Science
Break					
Venue: Multipurpose Hall		Poster Session			
Time					
Poster Session	17:00 ~ 18:00		Poster Session	*Posters must be attached in advance to the poster panel in the Multipurpose Hall. Poster locations are indicated by poster number. *Voting will be held for the best posters from the student poster session.	